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Sikkim Manipal University
Directorate of Distance Education

Model Question Paper

Subject Code: MT0041

Subject Name: Computer Organisation and Architecture

Credits: 4 **Marks: 140**

Part A (One mark questions)

1. Information fed to a computer can be categorized as ……..

a. either instructions or data.

b. instructions

c. data.

d. signal

2. A collection of lines that connects several devices is called ……

a. bus

b. peripheral connection wires

c. Both a and b

d. coaxial cable

3. PC Program Counter is also called……..

a. Instruction pointer

b. memory pointer

c. data counter

d. file pointer

4. When lower byte addresses are used for the more significant bytes (the leftmost bytes) of the word, this technique is called ……

a. little-endian

b. Addressing mode

c. big-endian

d. Both a and c

5. An Add instruction Add A, B which performs the operation B -> [A] + [B].In this instruction operand B work as ……..

a. Source

b. destination

c. Both a source and a destination.

d.general operand

6. In a single byte how many bits will be there ?

a. 8

b. 16

c.4

d. 32

7. The access time of memory is…….. ... The time required for performing any single CPU operation

a. Longer than

b. Shorter than

c. negligible than

d. same as

8. In two bus architecture all the register outputs are connected to ……..., and all register inputs are connected to ……...

a.CPU , ALU

b. out put device, input device

c. bus A, bus B.

d. motherboard, power supply

9. Memory address refers to the successive memory words and the machine is called as……

a. word addressable

b. byte addressable

c.bit addressable

d. Tera byte addressable

10. The time that elapses between the initiation of an operation and completion of that operation is called

a. throughput

b. memory response time.

c. memory access time.

d. Execution time

11. A semiconductor memory constructed using bipolar transistors or MOS transistor stores information in the form of a ……

a. Flip-flop voltage levels

b. bit

c. byte

d. opcodes values

12. A simple way of performing I/O tasks is to use a method known as ……

a. program-controlled I/O.

b.program-controlled input

c. Program-controlled output

d. I/O operation

13. Striking key stores the corresponding character code in an 8-bit buffer register associated with the keyboard. This register is called as ……..

a. DATAINOUT

b. DATAOUT

c. DATAIN

d. Both a and b

14. When the character is transferred to the processor, status control flag SIN is automatically cleared to …….

a. Zero

b. 1

c. 2

d. yes

15 .an exception conditions in a computer system caused by an event external to the CPU is called……..

a. Interrupt

b. halt

c. wait

d. process

16. When the CPU detects an interrupt, it then saves its ……...

a. Previous state

b. next state

c. Current state

d. both a and b

17. The easiest numbers to represent are the ……

a. non-negative integers

b. negative integers

c. Binary numbers

d. Rational Numbers

18. For addition If both numbers are positive and the result is negative, then report …….

a. underflow.

b. overflow.

c. Overflow as well as underflow

d. Error

19. A number which have a pair of integers, one for the numerator and one for the denominator is called

a. rational numbers

b. Binary number

c. hexa decimal number

d. decimal number

20. Booth's Algorithm Handles positive and negative numbers ……..

a. uniformly

b. differently

c. politely

d. asynchronously

21. Computer architecture has gone through …….. rather than …….. changes. fill up the blanks with one of the following combination.

a. Evolutional, Revolutional

b. revolutional, evolutional

c. revolutional, exceptional

d. exceptional, revolutional

22. SIMD stands for……..

a. single instruction stream over multiple data streams

b. single instruction stream over minimum data streams

c. single instruction stream over media data streams

d. multiple instruction streams and a single data stream

23. The major distinction between multiprocessors and multicomputer is…….

a. memory sharing and the mechanisms used for inter-processor communication.

b. Non memory sharing mechanism

c. processing method

d. execution time

24. A vector processor is equipped with …….

a. Multiple vector pipelines

b. single vector pipelines

c. commercial machines

d. graph

25. A pipeline is like ……..

a. an automobile assembly line

b. house pipeline

c. Both a and b

d. a gas line

26. Pipelining increases the CPU instruction ……

a. Throughput

b. efficiency

c. latency

d. both a and b

27. Data hazards occur when……

a. Greater performance loss

b. Pipeline changes the order of read/write accesses to operands

c. some functional unit is not fully pipelined

d. machine size is limited

28. The cost-performance ratio is a good indicator of……

a. relative quality

b. relative performance

c. relative quantity

d. both a and b

29. For the majority of the design space, cost and performance are treated together as a single parameter, called…….

a. the cost-performance ratio

b. the cost-analysis ratio

c. Both a and b

d. performance analysis

30 .The architects actually have control of both ……

a. algorithm and the architecture

b. algorithm and the programs

c. Hardware and software

d. hardware and algorithm

31. Select which of the following is the formula for measuring performance in MIPS .

a.MIPS = (instructions/cycle)(cycles/second) *10-6

b.MIPS = (instructions/cycle)(cycles/second) *10-4

c. MIPS = (10*instructions/cycle)(cycles/second) *10-6

d.MIPS = (instructions/cycle)(cycles/second) *10-7

32. CISC stands for……..

a. Complex instruction set computers

b. Complex instruction set compilers

c. Common instruction set computers

d. Compound instruction set computers

33. A vectorizing compiler would regenerate ……..lost in the use of sequential languages. select one of the following to fill the gap?

a. Parallelism

b. serialization

c. track

d. both a and b

34. Some degree of concurrent access can be achieved by partitioning the memory …….

a. at a given level into several modules

b. at any level into the single module

c. provide different memory

d. provide a large memory

35. DASDs stand for ……

a. direct-access storage devices

b. Derived - access storage devices

c. direct-accumulation starting devices

d. direct-access stimulation devices

36. The concurrency that is obtained when the same operation is applied to some or all elements of a data ensemble, process is called…….

a. data parallelism

b. data serialization

c. concurrency control

d. both a and b

37. For shared-memory-programming model, what is the advantage we have from the programmer's point of view?

a. the notion of data “ownership” is lacking, and hence there is no need to specify explicitly the communication of data from producers to consumers

b. Processor job will be easy

c. calculation of address will be easy

d. both b and c

38. The connection of two or more interconnection networks is called ……

a. intra networking

b. inter networking

c. wireless

d. LAN networking

39. Devices that are used primarily to transport data between the processor and the user are known as……..

a. data presentation device.

b. basic storage devices

c. networking devices.

d. data transfer device

40. The I/O processor (IOP) has a direct access to …….. And contains a number of independent data channels. Fill up the blanks with one of the following option.

a. main memory

b. secondary memory

c. cache

d. flash memory

Part B (Two mark questions)

41. **The unit which decodes and translates each instruction and generates the necessary enable signals for ALU and other units is called…….**

a. arithmetic unit

b. Logical unit

c. Control unit

d. CPU

42. Which of the following is not the Hardware Interrupt?

a. key pressed on the keyboard

b. a hard disk completing the reading or writing of data

c. the reception of an Ethernet packet

d. software generated events

43. Registers are used…….... in the processor during processing. which of the following is correct to fill the blanks

a. to store data temporarily

b. to store data permanently

c. Both a and b

d. to store processor clock cycles

44. In case of only one memory operand, When a second operand is needed, as in the case of an Add instruction, we use processor register called……..

a. source

b. register

c. operand

d. accumulator

45. The process by which, replacing the current contents of the PC by the branch address is called……

a. Addressing

b. Reallocation

c. Branching

d. Naming

46. A PLA consists of an array of ……..gates followed by an array of…….gates

a. NAND gates, OR gates

b. AND gates, XOR gates

c. OR gates, AND gates

d. AND gates, OR gates

47. DRAM memory cell uses a ……. and a ……... to store a bit of data.

a. capacitor and flip-flop

b. AND gates, XOR gates

c. 4-6 transistor, capacitor

d. single transistor, capacitor

48. Data transfer between the main memory and the CPU register takes place through two registers namely ……..

a. MAR and MDR

b. accumulator and program counter

c. general purpose register and MDR

d. MAR and Accumulator

49. Some memory address values are used to refer to peripheral device buffer registers, such as DATAIN and DATAOUT. such computers use an arrangement called memory-mapped I/O

a. memory-mapped OUTPUT

b. memory-mapped INPUT

c. memory-mapped I/O

d. memory-processor I/O

50. When the value in the current count register goes from 0 to -1, a terminal count (TC) signal is generated, which signifies the …….. of the DMA transfer sequence

A .clock

b. interrupt

c. starting

d. completion

51. value 1: 1 0 1 1
+ value 2: + 0 0 1 0
what will be the answer of above binary addition of two given values

a. 1 1 0 1

b.1 0 0 1

c.13

d. 1111

52. According to the Booth's Recoding Table if a is 00011110 , the recoded value of a is ……

a.00+1000+10

b.0010000

c. 00100010

d. 0 0 +1 0 0 0 -1 0

53. Memory-to-memory architecture supports …….

a. pipelined flow of vector operands directly from the memory to pipelines and then back to the memory

b. vector registers to interface between the memory and functional pipelines.

c. SIMD computers for synchronized vector processing

d. spatial parallelism rather than temporal parallelism

54. At the processor-level abstract architecture, we are concerned with……

a. programming model

b. hardware model

c. either the programming model or the hardware model of a particular processor.

d. Design

55. Control hazards can cause ……..

a. Structural Hazards

b. data hazards.

c. a greater performance loss than the data hazards.

d. Both a and b

56. The role of applications is critical in the high-performance arena because ……... to wring the greatest possible throughput from an architecture. Fill up the blanks with one of the following choice.

a. costs tend to be very low

b. costs tend to zero

c. costs tend to be very high

d. Both a and c

57. f3:V x V --> V

f4: V x S --> V

Which of the following operation is represented by mappings f3 and f4 ?

a. binary operations.

b. unary operation

c. f3 represents the unary operation where as f4 represents the binary operation

d. ternary operation

58. Which of the following are not components of the locality of reference, which coexist in an active process?

a. Overlay

b. temporal,

c. spatial

d. sequentially localities

59. The address mapping is done, when the program is initially loaded is called……..

a. dynamic relocation.

b. Relocation

c. static relocation

d. Dynamic as well as static relocation

60. The channel which handles the multiple requests and multiplexes the data transfers from these devices a byte at a time is known as …….

a. multiplexor channel

b. The selector channel

c. block multiplex channel

d. both a and c

Part C (Four mark questions)

61. State weather the following statement is true or false for PCI bus.

1). The PCI bus runs at 33 MHz and can transfer 32-bits of data (four bytes) every clock tick

2).The PCI interface chip may support the video adapter, the EIDE disk controller chip and may be two external adapter cards

3).PCI bus deliver the different throughout only on a 32-bit interface that other parts of the machine deliver through a 64-bit path.

a. 1. True, 2. True, 3. false

b. 1. True, 2. False, 3. false

c. 1. False, 2. False, 3. false

d. 1. True, 2. True, 3. true

62. State weather the following statement is true or false for three bus architecture. where we have consider the instruction to add content of memory location NUM to register R0.

1). Fetch the instruction.

2). Fetch the content of memory location pointed by the address field of the instruction.

3). Perform the addition and Load the result in R0.

a. 1. True, 2. True, 3. true

b. 1. True, 2. False, 3. false

c. 1. False, 2. False, 3. false

d. 1. True, 2. True, 3. false

63. Match the followings:

Part A

1). machines that store operands in pushdown stack.
2). The different ways in which the location of an operand is specified in an instruction
3). The operand is the contents of a processor register

Part B

A. addressing modes

B. Register mode

C. zero addresses instructions.

a. 1. C, 2. A, 3. B

b. 1.C, 2. B, 3. A

c. 1. A, 2. C, 3. B

d. 1.B, 2.A, 3. C

64. Match the followings:

Part A

1). A word whose individual bits represent the control signals.
2). A sequence of control words corresponding to the control sequence of a machine instruction constitutes the micro routine for that instruction.

3). A counter which is used to read the control words sequentially from the microprogram memory

Part B

A. Micro routine:

B. Control Word (CW):

C. Micro program Counter

a. 1. C, 2. A, 3. B

b. 1.C, 2. B, 3. A

c. 1. A, 2. C, 3. B

d. 1.B, 2.A, 3. C

65. Match the followings:

Part A

1). Both CPU and main memory are directly connected to the system bus
2). The communication between CPU and cache is through a separate bus, which is isolated from the main system bus

3). any main memory block can be loaded to any cache block position

Part B

A. Associative mapping technique

B. Control Word (CW):

C. Look-aside design

a. 1. C, 2. A, 3. B

b. 1.C, 2. B, 3. A

c. 1. A, 2. C, 3. B

d. 1.B, 2.A, 3. C

66. State weather the following statement is true or false for cache memory

1). It reduces the speed disparity between the CPU and main memory.

2). A cache serves as a buffer between a CPU and main memory

3). the time required to access the cache memory is greather than the time required to access main memory.

a. 1. True, 2. True, 3. true

b. 1. True, 2. False, 3. false

c. 1. False, 2. False, 3. false

d. 1. True, 2. True, 3. false

67. Match the followings:
Part A
1). interrupt will “identify" itself by sending information to the CPU.

2). a capability provided by some computer bus architectures that allows data to be sent directly from an attached device to the memory on the computer's motherboard

3). feature repeats the DMA transfer sequence by reloading the DMA channel's current registers from the base registers at the end of a DMA sequence and re-enabling the channel

Part B
A. vectored interrupts
B. auto initialization
C. Direct Memory Access (DMA)

a. 1. C, 2. A, 3. B

b. 1.C, 2. B, 3. A

c. 1. A, 2. C, 3. B

d. 1.B, 2.A, 3. C

68. State weather the following statement is true or false for DMA

1). DMA is fast because only one or two bus read/write cycles are required per piece of data transferred

2). DMA also off-loads the processor

3). data transfer is actually occurring in serial, thus decreasing overall system utilization.

a. 1. True, 2. True, 3. true

b. 1. True, 2. False, 3. false

c. 1. False, 2. False, 3. false

d. 1. True, 2. True, 3. false

69. Multiply 00101101(b) by 00011110 (a) using Booth's multiplication

a. 1|0000010101010111

b. 1|0000010101000111

c. 1|0000010101000110

d.100000010101000110

70. State weather the following statement is true or false for Functional parallelism?
1. Use multiple functional units simultaneously
2. Practice pipelining at various processing levels.
3. Pipelined instruction execution, pipelined arithmetic computations, and memory-access operations

a. 1. True, 2. true, 3. true

b. 1. true, 2. false, 3. false

c. 1. false, 2. false, 3. false

d. 1. true, 2. true, 3. false

71. State weather the following statement is true or false for Major Hurdle of pipelining

1. Structural hazards arise from resource conflicts when the hardware cannot support all possible combinations of instructions in simultaneous overlapped execution.

2. Data hazards arise when an instruction depends on the results of a previous instruction in a way that is exposed by the overlapping of instructions in the pipeline.

3. Control hazards arise from the pipelining of branches and other instructions that change the PC.

a. 1. True, 2. True, 3. true

b. 1. True, 2. False, 3. false

c. 1. False, 2. False, 3. false

d. 1. True, 2. True, 3. false

72. state weather the following statement is true or false for important ways to make architectural advances:

1.Make small perturbations in cost and performance that yield lower cost- performance ratios

2.just check their performence for the same input values.

3. Boost absolute performance to make new computations feasible at reasonable cost.

a. 1. True, 2. True, 3. true

b. 1. True, 2. False, 3. false

c. 1. False, 2. False, 3. false

d. 1. True, 2.false, 3. true

73. State weather the following statement is true or false for The instruction issue and dispatch.
1. Shelving is used , 'issue' refers to, the action of disseminating decoded independent instructions to the EUs

2. Shelving is not used, 'issue' designates the dissemination of decoded instructions to the shelving buffers.

3.in the case of shelving, dispatch designates the dissemination of dependency-free instructions from, the shelving buffers to the EUs.

a. 1. True, 2. True, 3. true

b. 1. True, 2. False, 3. false

c. 1. False, 2. False, 3. true

d. 1. True, 2. True, 3. false

74. State weather the following statement is true or false for Cache memory

1) Cache memories are high-speed buffers which are inserted between the processors and main memory

2.) They can also be inserted between main memory and mass storage.

3.) It can be used as secondary memory

a. 1. True, 2. True, 3. true

b. 1. True, 2. True, 3. false

c. 1. False, 2. False, 3. false

d. 1. False, 2. True, 3. false

75. State weather the following statement is true or false for problem in accessing data is to design a system that is efficient in:

1) Finding the physical location of the required data.

2.) Finding a path from the processor memory to the particular physical device that contains the information.

3.) It should provide the higher levels of the storage hierarchy

a. 1. True, 2. True, 3. true

B.1. false, 2. False, 3. false

c. 1. True, 2. True, 3. false

d. 1. False, 2. False, 3. false

Answer Keys

Part - A				Part - B		Part - C	
Q. No.	**Ans. Key**	**Q. No.**	**Ans. Key**	**Q. No.**	**Ans. Key**	**Q. No.**	**Ans. Key**
1	A	21	A	41	C	61	A
2	A	22	A	42	D	62	A
3	A	23	A	43	A	63	A
4	C	24	A	44	A	64	D
5	C	25	A	45	C	65	B
6	A	26	A	46	D	66	C
7	A	27	B	47	D	67	C
8	C	28	A	48	A	68	D
9	A	29	A	49	C	69	C

10	C	30	A	50	D	70	A
11	A	31	A	51	A	71	A
12	A	32	A	52	D	72	D
13	C	33	A	53	A	73	C
14	A	34	A	54	C	74	B
15	A	35	A	55	C	75	C
16	C	36	A	56	C		
17	A	37	A	57	A		
18	B	38	B	58	A		
19	A	39	A	59	C		
20	A	40	A	60	A		